REMARKS

Claims 1-6 and 8-13 stand rejected under 35 USC §102(e) as being anticipated by Mori (US 2002/0008278A1)

Claim 7 is rejected under 35 USC §103(a) as being unpatentable over Mori in view of Hayakawa (US 5,976,934).

Claims 1 and 12 are amended. No new subject matter is added. Claims 2 and 3 are cancelled. Claims 1 and 4-13 remain pending. Reconsideration of the pending claims is requested in light of the following remarks.

Claim Rejections – 35 USC § 102

Claims 1-6 and 8-13 are rejected under 35 USC §102(e) as being anticipated by Mori.

Claims 1 and 12 are amended to incorporate the limitations of claim 2 and claim 3. Claims 2 and 3 are cancelled. Amended claims 1 and 12 now recite that the claimed method further comprises "implanting impurity ions into the first and second active regions prior to formation of the tunnel oxide layer and the gate oxide layer."

Contrary to the recited limitation, Mori explains in [1024], first sentence, that "a tunnel oxide film 21a is *first* made as a gate insulating film" (emphasis added). Then, in [1024], fifth sentence, Mori teaches that "thermal oxidation is conducted to form a gate oxide film 21b necessary for a high-voltage circuit in the peripheral circuit region." Finally, in the last sentence of [1024] – "*Thereafter*, ion implantation is conducted in the peripheral circuit region for controlling the channel impurity concentration" (emphasis added).

It is clear from [1024] that Mori teaches away from the claimed invention by implanting impurity ions *after* formation of the tunnel oxide layer and the gate oxide layer (emphasis added). Consequently, Mori does not anticipate claim 3 because claim 3 recites implanting impurity ions prior to formation of the tunnel oxide layer and gate oxide layer. This limitation is set forth in the application as filed on page 6, lines 23-26.

Claims 1 and 12 are not anticipated by Mori for at least the reason given above. Claims 4-6, 8-11, and 13 are allowable for at least the same reason as claim 1.

Claim Rejections – 35 USC § 103

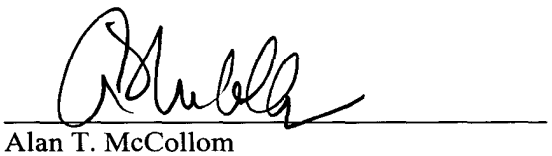
Claim 7 is rejected under 35 USC §103(a) as being unpatentable over Mori in view of Hayakawa. The applicant respectfully disagrees. Claim 7, because of its dependency on claim 1, is allowable for at least the same reason as claim 1.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1 and 4-13 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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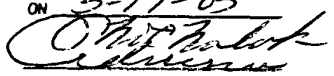

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) A method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising:

forming a device isolation layer at a predetermined region of a semiconductor substrate to define at least one first active region in the cell array region and a second active region in the peripheral circuit region;

forming a floating gate pattern covering the first active region and a gate conductive layer covering the peripheral circuit region;

forming a tunnel oxide layer interposed between the floating gate pattern and the first active region;

forming a gate oxide layer interposed between the gate conductive layer and the second active region;

implanting impurity ions into the first and second active regions prior to formation of the tunnel oxide layer and the gate oxide layer;

sequentially forming an inter-gate dielectric layer and a control gate conductive layer on an entire surface of the substrate having the floating gate pattern and the gate conductive layer; and

selectively removing the control gate conductive layer and the inter-gate dielectric layer which are located in the peripheral circuit region, thereby exposing the gate conductive layer in the peripheral circuit region.

2. (Cancelled)

3. (Cancelled)

12. (Amended) A method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising:

forming a device isolation layer at a predetermined region of a semiconductor substrate to define at least one first active region in the cell array region and a second active region in the peripheral circuit region;

forming a floating gate pattern covering the first active region and a gate conductive layer covering the peripheral circuit region;

forming a tunnel oxide layer interposed between the floating gate pattern and the first active region;

forming a gate oxide layer interposed between the gate conductive layer and the second active region;

implanting impurity ions into the first and second active regions prior to formation of the tunnel oxide layer and the gate oxide layer;

sequentially forming an inter-gate dielectric layer and a control gate conductive layer on an entire surface of the substrate having the floating gate pattern and the gate conductive layer; and

stripping the control gate conductive layer and the inter-gate dielectric layer in the peripheral circuit region to expose the gate conductive layer in the peripheral circuit region.